Sayed Shakir Hussain

PROCESS ENGINEER – Process Optimization, Root Cause Analysis, Documentation Control

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SKILLS

- **Process Optimization**: Lean Manufacturing, Six Sigma, Cycle Time Reduction, and Bottleneck Elimination.
- **Technical Tools**: MATLAB, Simulink, AutoCAD, OrCAD, Excel (VBA, PivotTables), Agile PLM, and Visio.
- **Data & Analysis**: Root Cause Analysis, FMEA, Control Charts, Pareto, Histogram, and Capability Studies.
- **Quality & Compliance**: ISO 9001, IPC-A-610, CE, IEC Standards, Internal Audits, Documentation, SOPs.
- **Project Execution**: Cross-functional Coordination, MS Project, Jira, Timeline Control, and Risk Reporting.

WORK EXPERIENCE

Senior Engineer – Process Engineering **August 2015 – July 2022**
Flex *India*

- Saved $1.05M annually by applying teardown analysis and alternate sourcing across 13 electronic devices during cost-down projects involving component evaluation, supplier review, and functional equivalency validation tasks.
- Facilitated 6 industrial Kaizen workshops that improved process sequences, corrected assembly errors, standardized tool layouts, and delivered 50% cycle time reduction across 4 concurrent production improvement initiatives.
- Prepared 48 process-specific process guides in 30 days to support transfer builds, enabling error reduction by 40% across two assembly lines through better operator guidance, sequence clarity, visual inspection alignment.
- Executed 4 on-site assignments at US facilities supporting NPI builds across telecom, medical, automotive, and consumer product lines, delivering fixture tuning, test setup optimization, and early defect containment reviews.
- Processed 2,500+ ECOs using Agile PLM by validating specifications, updating BOMs, reviewing revision histories, flagging mismatches, and confirming proper alignment with process constraints and tooling dependencies.
- Improved throughput by 34% across two production cells by balancing operator distribution, modifying layout paths, eliminating double-handling zones, and synchronizing part supply with workstation loading sequences.
- Reduced scrap by 53% by isolating key root causes linked to fixture wear, test variability, and incorrect parameter setups, followed by corrective action deployment and revised setup sheet revision across impacted assembly cells.
- Introduced visual quality checkpoints for 7 product variants by integrating defect tags, rework flags, and traceable issue logs into the existing MES, boosting inline quality alert responsiveness and lowering escape rate by 37%.

New Product Development Engineer **January 2013 – August 2015**
Ready LED Lighting Pvt.Ltd. *India*

- Designed 20+ LED drivers using buck and flyback topologies; aligned thermal constraints with PCB layout guidelines and enclosure design rules to meet electrical, mechanical, reliability targets across 5 product models.
- Issued 80+ structured BOMs and workflow steps across 3 lighting product families, resulting in a 29% drop in rework errors over three shifts by tightening process flow, visual references, and part traceability standards.
- Completed LM79 testing for 18 luminaires and resolved 12 nonconformities by iterating reflector angles, optical lens curvature, LED mounting, and shielding, aligning results with IES test reports and lumen efficacy thresholds.
- Reduced field returns by $24K after isolating ESR drift in 5 high-failure SKUs through 48-hour thermal burn-in tests, waveform logging, component sourcing review, improving circuit stability and pass rates under real load.
- Decreased PCB redesign frequency by 60% through corrective updates to pin mappings, trace geometries, copper path balancing, thermal region resizing, enhancing manufacturability and testability across three lighting lines.
- Secured UL, CE, and BIS certifications for 12 SKUs by modifying plastic enclosures, increasing creepage and clearance margins, and coordinating test sequences across accredited labs, aligning with three compliance reports.
- Verified 100+ LED array designs by analyzing forward voltage spread, junction temperature rise, ESR instability, and copper trace drop, improving consistency in brightness, color rendering, and board-level thermal behavior.
- Optimized dimmer compatibility across 8 LED driver variants by tuning startup currents, minimizing flicker, and synchronizing TRIAC response curves, reducing complaints and ensuring lumen output under variable loads.

EDUCATION

Master of Engineering – Electrical and Computer **April 2025**
Carleton University, Ontario

Bachelor of Technology – Electronics & Communication Engineering **May 2013**
Vel Tech University, India

Diploma – Electronics & Telecommunication Engineering **December 2009**
State Council for Technical Education, Silchar, India

CERTIFICATIONS

- **Lean Green Belt** – Flex
- **Certified Internal Auditor** – BMQR
- **Diploma in Robotics** – ThinksLab